



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,492	07/05/2007	Hani Achkar	2085.006US1	1933
21186	7590	04/15/2008		
SCHWEGMAN, LUNDBERG & WOESSNER, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			EXAMINER	
		HENSON, MISCHITAL		
		ART UNIT	PAPER NUMBER	
		4146		
		MAIL DATE	DELIVERY MODE	
		04/15/2008	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/591,492	Applicant(s) ACHKAR ET AL.
	Examiner Mi'schita Henson	Art Unit 4146

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 01 September 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-26 and 29-38 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7,15,17-24 and 29-38 is/are rejected.
 7) Claim(s) 8-14,16 and 25-26 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 01 September 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) *Notice of Draftsperson's Patent Drawing Review (PTO-544)*
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 01 September 2006.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Acknowledgment

2. Acknowledgment of the cancellation of claims 27 and 28 in the Preliminary Amendment filed September 1, 2006 is hereby made.

Claim Objections

3. Claims 3-6, 30-31, 33-34 and 37 are objected to because of the following typographical errors:

- a. In claim 3: "processing device; and an industrial" should be -processing device; or an industrial-.
- b. In claim 4: "processing device; and an industrial" should be -processing device; or an industrial-.
- c. In claim 5: "test vectors, and; a predetermined delay" should be -test vectors or a predetermined delay-.

- d. In claim 6: "Active-X; and a serial communication" should be -Active-X; or a serial communication-.
 - e. In claim 30: "system of claim 27" should be -system of claim 29-.
 - f. In claim 31: "system of claim 28" should be -system of claim 30-
 - g. In claim 33: "process of claim 30" should be -process of claim 32-
 - h. In claim 34: "process of claim 31" should be -process of claim 33-
 - i. In claim 37: "apparatus of claim 34" should be -apparatus of claim 36-
- Appropriate correction is required.
4. Claim 16 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim must refer back to more than one preceding independent or dependent claim in the alternative. See MPEP § 608.01(n). Accordingly, the claim 16 has not been further treated on the merits.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 20-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 20-24 are directed to a data format which does not fall under one of the statutory subject matter categories.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 5 and 38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 5, the phrase "predefined timing reference may comprise" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 2, 29, 32 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Ricchetti et al. in WO 03/048794 A1.

Regarding claim 1, Ricchetti et al. teaches:

A logical connection port (the port means by which the embedded BIST controller connects to the external connector is interpreted to be a logical connection port, see external connector, page 10 lines 26-27 and ECE_N in Figure 5) for an embedded device testing system (the embedded electronic system Built-In Self-Test controller is interpreted to be an embedded device testing system, see page 7, lines 1-3), the testing system comprising apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs (the means for comparing the actual scan-out values to expected scan-out values is interpreted to be

the apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, where the actual scan-out values are interpreted to be input/output vectors of the actual device under test and the expected scan-out values are interpreted to be from the modelled DUT, see page 8, lines 23-30), wherein the logical connection port is adapted to indicate a predefined timing reference (the Memory Delay is interpreted to be a predefined timing reference, see page 16 lines 1-4) for determining a point in time at which to sample an output vector as the corresponding output vector in an input/output vector pair.

Regarding claim 2, Ricchetti et al. teaches:

The logical connection port of claim 1 wherein the logical connection port resides in a DUT model (ECE_N is interpreted to be the logical connection port that resides in a DUT model, see ECE_N in Figure 5).

Regarding claim 29, Ricchetti et al. teaches:

An embedded device testing system (the embedded electronic system Built-In Self-Test controller is interpreted to be an embedded device testing system, see page 7, lines 1-3) for comparing actual device under test input/output vector pairs with modelled device under test input/output vector pairs (the means for comparing the actual scan-out values to expected scan-out values is interpreted to be the apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, where the actual scan-out values are interpreted to be input/output vectors of the actual device under test and the expected scan-out values are interpreted to be from the modelled DUT, see page 8, lines 23-30), wherein actual

device under test output vectors are sampled in accordance with a predefined timing reference (the Memory Delay is interpreted to be a predefined timing reference, see page 16 lines 1-4).

Regarding claim 32, Ricchetti et al. teaches:

A process for testing an embedded device under test, including the steps of: comparing actual device under test input/output vector pairs with modelled device under test input/output vector pairs (the means for comparing the actual scan-out values to expected scan-out values is interpreted to be comparing the actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, where the actual scan-out values are interpreted to be input/output vectors of the actual device under test and the expected scan-out values are interpreted to be from the modelled DUT, see page 8, lines 23-30), wherein actual device under test output vectors are sampled in accordance with a predefined timing reference (the Memory Delay is interpreted to be a predefined timing reference, see page 16 lines 1-4).

Regarding claim 35, Ricchetti et al. teaches:

Apparatus for testing a device under test (the embedded electronic system Built-In Self-Test controller is interpreted to be an apparatus for testing a device, see page 7, lines 1-3), including:

- (a) means for applying a test input vector (the means for apply scan vectors is interpreted to be a means for applying a test input vector, page 11, lines 27-29) to the device under test; and
- (b) means for sampling an output vector (the means for applying the Memory Delay is

interpreted to be a means for sampling, page 15, lines 22-24) from the device under test in response to said input vector, wherein the wherein said sampling is effected in accordance with a predefined timing reference.

10. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Lottridge et al. in US Patent 5,796,750.

A generic test execution engine for testing (the automatic tester is interpreted to be a generic test execution engine, see Abstract) at least one embedded DUT comprising:

(a) a test vector interface (the in-system programming interface is interpreted to be the test vector interface, see column 3 lines 63-64) comprising parsing means (the compiler is interpreted to have a parsing means, see compiler, column 4 lines 39-41) for parsing modelled output test vectors with predefined input test vectors in accordance with a predefined timing reference to determine a test vector file comprising pairs of corresponding stabilised input and output test vectors;

(b) a DUT interface (the connector is interpreted to be a DUT interface, see column 4, lines 64-67) comprising addressing means (the parallel port is interpreted to be an addressing means, see parallel port, column 4 lines 9-10) for addressing, via data ports, test vectors to respective DUT's in accordance with an address identifier within the test vector file, and communication means (the means for receiving the generic vector file that is output by program isp_prog() is interpreted to be a communication means, see generic vector file, column 3 lines 13-15) for receiving DUT output vectors in response to the test vectors;

(c) a test result interface (the user interface is interpreted to be a test result interface, column 4, line 44) comprising processing means (the microprocessor is interpreted to be a processing means, see microprocessor, column 3 line 57) for processing respective pairs of stabilised input and output test vectors and corresponding received DUT output vectors.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ricchetti et al. in WO 03/048794 A1 as applied to claim 1 above, in view of Oke et al. in US Patent 5,642,057 (as best understood).

Ricchetti et al. teach the limitations of claim 1 as indicated above. Ricchetti et al. differs from the claimed invention in that it is silent on having a modelled vector of the specified device type.

Oke et al. teaches "test vectors that have already been developed" (test vectors that have already been developed are interpreted to be modeled vectors, see Abstract) for stand alone microprocessors and one of ordinary skill in the art would understand that any device under test (i.e. smoke, fire, security, medical, biological or industrial devices) having a microprocessor utilizing test vectors would use a device specified

Art Unit: 4146

modelled vector to compare the actual output vector in order to determine failures, signal differences, etc. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Oke et al. in the system of Ricchetti et al. because it is well known in the art to use a modelled test vector as the threshold and/or limitation vector to compare the actual output vector when testing a DUT, thereby improving the functionality of the system.

13. Claims 5, 30-31, 33-34 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ricchetti et al. in WO 03/048794 A1 as applied to claims 1, 29, 32 and 35 above, in view of Potts et al. in US Patent 5,663,879 (as best understood).

Ricchetti et al. teach the limitations of claims 1, 29, 32 and 35 as indicated above. Ricchetti et al. differs from the claimed invention in that it is silent on having a predefined timing reference with a delay period.

Potts et al. teach a predetermined signal event used as a timing reference (the predetermined signal event is interpreted to be a predefined timing reference, see Abstract) for a test event of an integrated circuit. Potts et al. also discloses an output based upon an input affected by some variable delay (see column 2 lines 1-8). One of ordinary skill in the art would comprehend that delay length is variable and can be set to any length of time that is suitable to the current application (i.e. the length of time before the corresponding output vector stabilizes). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Potts et al. in the system of Ricchetti et al. because Potts et al. discloses

the fixed reference method as the "standard approach to vector generation and testing" (see column 2 lines 14-15), thereby improving the functionality of the system.

14. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan et al. in US Patent 6,950,771, in view of Lottridge et al. in US Patent 5,796,750.

Fan et. al discloses applying test vectors to a device for testing purposes (column 5 lines 60-64) utilizing first, second, and third data sets (see claims 1, 2 and 10). Fan et al. also discloses comparing the data sets (see "identifying correspondences" in claim 1 and comparing in claim 2). One of ordinary skill would understand that it is necessary to determine a test configuration parameter applicable to testing the DUT, utilizing and processing test vectors as inputs results in test vector outputs and matching the test vectors accordingly, initial data sets can be determined from any reliable source (i.e. the configuration parameter set), data sets can be compared in any order suitable to the application, and the results need to be communicated in some manner.

Lottridge et al. teaches a system with a compiler (the compiler is interpreted to have a parsing means, see compiler, column 4 lines 39-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Lottridge et al. in the system of Fan et al. because it is well known in the art that a parser is a component of a compiler.

15. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lottridge et al. in US Patent 5,796,750 as applied to claim 15 above, in view of Oke et al. in US Patent 5,642,057.

Lottridge et al. teach the limitations of claim 15 as indicated above. Lottridge et al. differs from the claimed invention in that it is silent on having a modelled vector of the specified device type.

Oke et al. teaches "test vectors that have already been developed" (test vectors that have already been developed are interpreted to be modeled vectors, see Abstract) for stand alone microprocessors and it and of ordinary skill in the art would understand that any device under test (i.e. smoke, fire, security, medical, biological or industrial devices) having a microprocessor utilizing test vectors would use a device specified modelled vector to compare the actual output vector in order to determine failures, signal differences, etc. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Oke et al. in the system of Lottridge et al. because it is well known in the art to use a modelled test vector as the threshold and/or limitation vector to compare the actual output vector when testing a DUT, thereby improving the functionality of the system.

16. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lottridge et al. in US Patent 5,796,750 as applied to claim 15 above, in view of Hatfield et al. in US Patent 5,920,830.

Lottridge et al. teach the limitations of claim 15 as indicated above. Lottridge et al. differs from the claimed invention in that it is silent on having a logging means. Hatfield et al. teaches a method and apparatus for generating test vectors for use in testing utilizing a comparison program (the comparison program is interpreted to be a logging means, see Abstract and column 2 lines 10-12 and 29-31, column 3 lines 21-25)

for comparing outputs. Hatfield et al. also teach comparison program to create a report file (the report file is interpreted to be a formatted file, column 4 lines 56-57 that is formatted by a report generator, column 8 lines 28-30). One of ordinary skill would recognize that a file can be formatted to comprise of various fields suitable to the application. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Hatfield et al. in the system of Lottridge et al. because Hatfield teaches this method to increase the functionality of the system and reduce timing errors (see column 1 lines 60-63).

17. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ricchetti et al. in WO 03/048794 A1 and Oke et al. in US Patent 5,642,057 and further in view of Potts et al. in US Patent 5,663,879 (as best understood).

Ricchetti et al. teach a logical connection port (the port means by which the embedded BIST controller connects to the external connector is interpreted to be a logical connection port, see external connector, page 10 lines 26-27 and ECE_N in Figure 5) for an embedded device testing system (the embedded electronic system Built-In Self-Test controller is interpreted to be an embedded device testing system, see page 7, lines 1-3), the testing system comprising apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs (the means for comparing the actual scan-out values to expected scan-out values is interpreted to be the apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, where the actual scan-out values are interpreted to be input/output vectors of the actual device under test

and the expected scan-out values are interpreted to be from the modelled DUT, see page 8, lines 23-30), wherein the logical connection port is adapted to indicate a predefined timing reference (the Memory Delay is interpreted to be a predefined timing reference, see page 16 lines 1-4) for determining a point in time at which to sample an output vector as the corresponding output vector in an input/output vector pair.

Ricchetti et al. differs from the claimed invention in that it is silent on having a modelled vector of the specified device type and on having a predefined timing reference with a delay period.

Oke et al. teaches "test vectors that have already been developed" (test vectors that have already been developed are interpreted to be modeled vectors, see Abstract) for stand alone microprocessors and one of ordinary skill in the art would understand that any device under test (i.e. smoke, fire, security, medical, biological or industrial devices) having a microprocessor utilizing test vectors would use a device specified modelled vector to compare the actual output vector in order to determine failures, signal differences, etc.

Potts et al. teach a predetermined signal event used as a timing reference (the predetermined signal event is interpreted to be a predefined timing reference, see Abstract) for a test event of an integrated circuit. Potts et al. also discloses an output based upon an input affected by some variable delay (see column 2 lines 1-8). One of ordinary skill in the art would comprehend that delay length is variable and can be set to any length of time that is suitable to the current application (i.e. the length of time before the corresponding output vector stabilizes).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Oke et al. and Potts et al. in the system of Ricchetti et al. because it is well known in the art to use a modelled test vector as the threshold and/or limitation vector to compare the actual output vector when testing a DUT and Potts et al. discloses the fixed reference method as the "standard approach to vector generation and testing" (see column 2 lines 14-15), thereby improving the functionality of the system.

Allowable Subject Matter

18. Claims 8-14 and 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mi'schita' Henson whose telephone number is (571) 270-3944. The examiner can normally be reached on Monday - Thursday 7:30 a.m. - 4:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571) 272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 4146

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

m.h.
4/11/08

/Marvin M. Lateef/

Supervisory Patent Examiner, Art Unit 4146